AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

1. **(Previously Presented)** An integrated circuit for use in a transceiver module, the integrated circuit comprising:

a first electrical input port for receiving a first serial electrical data stream;

receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;

a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

receiver bypass circuitry for switchably selecting, based on a data rate of the first electrical data stream, a bypass data path from the first electrical input port to the first electrical output port to bypass retiming and reshaping of the first serial electrical data stream;

a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;

transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and

a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.

2. **(Original)** The integrated circuit of claim 1 wherein the bypass data path is selected when the first serial electrical data stream has a data rate below a predetermined threshold.

3. **(Original)** The integrated circuit of claim 2 wherein:

the receiver eye opener circuitry has a data rata range including 10 Gb/s; and

the bypass data path is selected when the first serial electrical data stream has a data rate below approximately 3 Gb/s.

4. **(Original)** The integrated circuit of claim 1 wherein the bypass data path is selected when the first serial electrical data stream has a data rate that is not within a data rate range of the receiver eye opener circuitry.

5-7. **(Canceled)**

8. **(Original)** The integrated circuit of claim 1 further comprising:

bypass control circuitry coupled to the receiver bypass circuitry for controlling the receiver bypass circuitry to select and deselect the bypass data path

9. **(Original)** The integrated circuit of claim 1 wherein the receiver bypass circuitry comprises an adaptive equalizer.

10. **(Original)** The integrated circuit of claim 1 further comprising:

power management circuitry for powering down the receiver bypass circuitry when the bypass data path is not selected.

11. **(Previously Presented)** In an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

switchably selecting or not selecting a bypass data path based on a data rate of the first electrical data stream;

retiming and reshaping the first serial electrical data stream when the bypass data path is not selected;

passing through the first serial electrical data stream when the bypass data path is selected;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit when the bypass data path is not selected, or transmitting the passed-through first serial electrical data stream to external to the integrated circuit when the bypass data path is selected;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and

transmitting the retimed and reshaped second serial electrical data stream.

12. **(Original)** The method of claim 11 wherein the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate below a predetermined threshold.

13. **(Original)** The method of claim 11 wherein the step of switchably selecting or not selecting a bypass data path comprises selecting the bypass data path when the first serial electrical data stream has a data rate that is not within a data rate range of the step of retiming and reshaping.

14. **(Canceled)**

15. **(Canceled)**

16. – 23. **(Canceled)**

24. **(Previously Presented)** A transceiver module, comprising:

a ROSA;

a TOSA;

receive path eye opener circuitry including a first input and output and configured so that a first data stream received from the ROSA has a lower jitter at the first output than at the first input;

receive path bypass circuitry configured so that when the first data stream has a data rate less than about 10Gb/s, the first data stream bypasses the receive path eye opener circuitry along a first bypass path;

transmit path eye opener circuitry including a second input and output and configured so that a second data stream has a lower jitter at the second output than at the second input; and

transmit path bypass circuitry configured so that when the second data stream has a data rate less than about 10Gb/s, the second data stream bypasses the transmit path eye opener circuitry along a second bypass path, the second bypass path being in communication with the TOSA.

25. **(Previously Presented)** The transceiver module as recited in claim 24, wherein the transceiver module is substantially compliant with the XFP MSA.

26. **(Previously Presented)** The transceiver module as recited in claim 24, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs at a data rate of about 8.5Gb/s.

27. **(Previously Presented)** The transceiver module as recited in claim 24, wherein at least one of the receive path bypass circuitry and the transmit path bypass circuitry comprises:

a CDR; and

a retimer.

28. **(Previously Presented)** The transceiver module as recited in claim 24, wherein at least one of the receive path bypass circuitry and the transmit path bypass circuitry comprises one of: a passive equalization circuit; and, an active equalization circuit.

29. **(Previously Presented)** The transceiver module as recited in claim 24, wherein the transmit path eye opener circuitry and the receive path eye opener circuitry are data rate responsive.

30. **(Previously Presented)** The transceiver module as recited in claim 24, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry can be implemented in at least one of the following ways: manually; and, automatically.

31. **(Previously Presented)** The transceiver module as recited in claim 24, wherein the receive path bypass circuitry is further configured so that the first data stream bypasses the receive path eye opener circuitry based on at least one of a loss of lock (LOL) signal and a loss of signal (LOS) signal.

32. **(Previously Presented)** The transceiver module as recited in claim 24, wherein:

the receive path eye opener circuitry and receive path bypass circuitry collectively comprise a receiver eye opener IC; and

the transmit path eye opener circuitry and transmit path bypass circuitry collectively comprise a transmitter eye opener IC.

33. **(Previously Presented)** The transceiver module as recited in claim 32, wherein the receiver eye opener IC and transmitter eye opener IC each comprise circuitry for a plurality of eye openers, each of the plurality of eye openers being configured to operate in connection with a predetermined data rate or predetermined range of data rates.

34. **(Previously Presented)** The transceiver module as recited in claim 24, wherein the transceiver module is compatible with the Fibre Channel protocol.

35. **(Previously Presented)** A transceiver module, comprising:

a ROSA;

a TOSA;

receive path eye opener circuitry including a first input and output and configured so that a first serial data stream received from the ROSA has a lower jitter at the first output than at the first input;

receive path bypass circuitry configured so that when the first serial electrical data stream has a data rate below a predetermined threshold, the first serial data stream bypasses the receive path eye opener circuitry along a first bypass path;

transmit path eye opener circuitry including a second input and output and configured so that a second serial data stream has a lower jitter at the second output than at the second input; and

transmit path bypass circuitry configured so that when the second serial data stream has a data rate below a predetermined threshold, the second serial data stream bypasses the transmit path eye opener circuitry along a second bypass path, the second bypass path being in communication with the TOSA, and the transceiver module being substantially compliant with the XFP MSA.

36. **(Previously Presented)** The transceiver module as recited in claim 35, wherein the transceiver module is compatible with the Fibre Channel protocol.

37. **(Previously Presented)** The transceiver module as recited in claim 35, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry can be implemented in at least one of the following ways: manually; and, automatically.

38. **(Canceled)**

39. **(Previously Presented)** A transceiver module, comprising:

a ROSA and a TOSA; and

a first IC configured to communicate with the ROSA, and a second IC configured to communicate with the TOSA, each IC configured to bypass clock and data recovery and retiming for a data rate of about 8.5Gb/s, and comprising:

a first buffer including a reference clock input and output;

a second buffer including data signal input and output, and an LOS output;

a CDR including:

a data signal input and output, the CDR data signal input connected to the second buffer data signal output;

reference clock input and output, the CDR reference clock input being connected to the first buffer reference clock output; and

an LOL output;

an RT including:

a reference clock input connected to the CDR reference clock output;

a data signal input connected to the CDR data signal output; and

a data signal output;

a multiplexer including:

a first input connected to the data signal output of the second buffer;

a second input connected to the RT data signal output;

a third input; and

an output;

a third buffer including:

an input connected to the multiplexer output; and

an output; and

a control logic module including:

a first input connected to the LOS output;

a second input connected to the LOL output;

a third input connectible to an external device;

a first output connectible to an external device; and

a second output connected to the third input of the multiplexer.

40. **(Previously Presented)** The transceiver module as recited in claim 39, wherein:

the control logic module is responsive to:

an LOS signal from the second buffer;

an LOL signal from the CDR; and

a command from a host; and

the control logic module is configured to transmit a control signal to the multiplexer.

41. **(Previously Presented)** The transceiver module as recited in claim 39, wherein the transceiver module is substantially compliant with the XFP MSA.

42. **(Previously Presented)** The transceiver module as recited in claim 39, wherein bypass of the receive path eye opener circuitry and transmit path eye opener circuitry occurs for at least one other data rate in addition to the about 8.5Gb/s data rate.

43. **(Previously Presented)** The transceiver module as recited in claim 39, wherein the transceiver module is compatible with the Fibre Channel protocol.